IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant(s): Robbe et al.

Serial No.: 10/556,647

Filed: November 10, 2005

For: Voltage Shift Control Circuit for PPL

Group Art Unit: 2816

Examiner: Khareem E. Almo

Docket No.: 28944/40163

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April 17, 2009

J. William Frank
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APPEAL BRIEF

Mail Stop Appeal Brief-Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal brief is filed in response to the final Office action dated August 7, 2008, and pursuant to the Notice of Panel Decision from Pre-Appeal Brief Review, mailed March 18, 2009.

(1) Real party in interest

This appeal is made on behalf of EADS Telecom, Rue Jean-Pierre Timbaud, Batiment Jean-Pierre Timbaud, Montigny Le Bretonneux 78180, France, as owner of the complete interest in the instant application.

(2) Related appeals and interferences

At present, there are no other appeals, judicial proceedings, or interferences known to the appellant, the appellant's legal representative, or the assignee which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

(3) Status of claims

Claims 1-5 and 7-14 stand finally rejected. Claim 6 has been objected to.

At issue on this appeal is the final rejection of claims 1-5 and 7-14.

(4) Status of amendments

The claims stand as presented by Amendment A filed March 25, 2008.

(5) Summary of the claimed subject matter

Independent claim 1 recites a voltage shift control circuit (50) intended to be placed in parallel with at least one series voltage shift capacitor (Ca) coupling the phase comparator (10) and the voltage controlled oscillator (30) of a phase locked loop (*see* page 4, lines 20-32, page 5, lines 4-12, and FIGS. 2 and 6). The voltage shift control circuit (50) comprises an input (21) intended to be coupled with the output of the phase comparator (10) and an output (22) intended to be coupled with the input of the voltage controlled oscillator (30) (*see* FIG. 2 and page 4, lines 28-32).

Further, the voltage shift control circuit (50) comprises various means plus function limitations: controlled charging means (51) designed to charge the voltage shift capacitor (Ca) according to a control signal (*see* page 6, line 13 to page 7, line 26 and FIG. 2), controlled pre-charging means (52) designed to accelerate the charging of the voltage shift capacitor (Ca) by the controlled charging means (51) (*see* page 7, line 27 to page 8, line 8 and FIGS. 2, 3, and 4), and controlled polarization means (53) designed to ensure the polarization of the input (21) during the pre-charging of the voltage shift capacitor (Ca) (*see* page 5, line 31 to page 6, line 12 and FIG. 2).

In one embodiment according to page 6, line 13 to page 7, line 26 and FIG. 2, the controlled charging means (51) comprises an operational transconductance amplifier (OTA1) connected as a voltage follower in parallel with the voltage shift capacitor (Ca). The controlled charging means (51) also comprises a controlled current source (CSa) connected between a terminal (Vss) and an inverting input of the operational amplifier (OTA1), this input is also looped to the output of the operational amplifier (OTA1) via a resistor (Ra). The output of the

operational amplifier (OTA1) is connected to the output (22) of the circuit (50) through a resistor (Rb). The non-inverting input of the operational amplifier (OTA1) is connected to the input (21) of the circuit (50) and also to the output of an operational amplifier (OTA2) of the controlled polarization means (53) via a switch (SW5).

Further, in another embodiment according to page 7, line 27 to page 8, line 8 and FIGS. 2, 3, and 4, the controlled pre-charging means (52) comprises a push-pull stage formed from two transistors (P3 and P4), which are a PMOS transistor and an NMOS transistor respectively, placed in series between terminals (Vdd and Vss). The control gates of the transistors (P3-P4) are connected to control gates of corresponding transistors of a push-pull output stage of the operational amplifier (OTA1) through controlled switches (SW1 and SW2), respectively. The closing of the switches (SW1-SW2) is controlled by a control signal (CTRL1) generated by a logic unit (54). The output of the push-pull stage (P3-P4) is connected to the output (22) of the circuit (50). Still further, FIG. 4 illustrates a coupling of the pre-charging means (52) with the operational amplifier (OTA1). The operational amplifier (OTA1) is represented in FIG. 4 by a differential amplifier followed by a push-pull output stage composed of two transistors (P1 and P2), that are a PMOS transistor and an NMOS transistor respectively, in series between the terminals (Vdd-Vss). The push-pull output stage (P1-P2) is connected to one end of the resistor (Rb), the other end of which is connected to the output of the push-pull stage (P3-P4) of the pre-charging means (52). The control gates of the transistors (P3-P4) are connected to the control gates of the transistors (P1-P2) by the switches (SW1-SW2), respectively. Further, a switch (SW7) can be coupled in parallel with the resistor (Rb) and switches (SW3 and SW4) can be placed between the gate of the transistor (P3) and the terminal (Vdd) and between the gate of the

transistor (P4) and the terminal (Vss), respectively. The switch (SW7) is controlled by the control signal (CTRL1) and the switches (SW3-SW4) are controlled by a signal corresponding to the inverse of the control signal (CTRL1).

In yet another embodiment according to page 5, line 31 to page 6, line 12 and FIG. 2, the controlled polarization means (53) can comprise an operational amplifier (OTA2) connected as a voltage follower. A non-inverting input of the operational amplifier (OTA2) receives a common mode voltage generated by a resistive bridge comprising two identical resistors connected in series between the terminals (Vdd and Vss). The inverting input of the operational amplifier (OTA2) is connected to the input (21) through a control switch (SW5). The switch (SW5) is controlled by a control signal (CTRL2) generated by the logic unit (54).

(6) Grounds of rejection to be reviewed on appeal

Applicants request review of the following grounds of rejection on appeal:

whether claims 1, 7, and 10-14 are obvious over Fan U.S. Patent No. 6,693,494 ("Fan") in view of Nilson and Riedel, Electric Circuits Fifth Edition, Figure 6.17 at pg. 227 ("Riedel"); and

whether claims 2-5, 8, and 9 are obvious over Fan in view of Kumar et al. U.S. Patent No. 6,611,161 ("Kumar") and further in view of Riedel.

(7) Argument

A. Claim 1, 7, and 10-14 are not obvious over Fan in view of Riedel because Fan and Riedel do not disclose or suggest at least one series voltage shift capacitor coupling a phase comparator and a voltage controlled oscillator of a phase locked loop.

The final Office action rejects claims 1, 7, and 10-14 under 35 U.S.C. § 103, as being unpatentable over Fan in view of Riedel. This rejection is improper because the applied references do not disclose or suggest the limitation in claim 1 of "at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop." The quoted language from claim 1 clearly states that the capacitor is coupled in series between the phase comparator and the voltage controlled oscillator of a phase locked loop. This is how a person of ordinary skill would interpret the language from claim 1.

Fan discloses a sigma delta fractional-N synthesizer (20) that includes a phase/frequency detector ("PFD") (21), charge pumps (27, 28, 29), a lowpass filter (29/129)[1], a loop filter (22), and a voltage controlled oscillator (23) in a main path, and a fractional-N divider (24) and a sigma delta calculator (25) in a return path. Referring to FIG. 6, the charge pumps (27, 28, 29) are coupled to the loop filter (22), which includes resistors (R1, R3) and capacitors (C1, C2, C3). The capacitors (C1, C2, C3) of the loop filter (22) are coupled between an input of the VCO (23) and ground, i.e., the capacitors (C1, C2, C3) are connected in parallel with the PFD (21) and the VCO (23). Fan does not disclose any other relevant capacitances.

In rejecting claims 1, 7, and 10-14 under 35 U.S.C. §103(a) as obvious over Fan in view of page 227 Riedel, the examiner admits that Fan "fails to disclose at least one series voltage shift capacitor." Office action at page 3. The examiner then introduces Riedel to supply the admitted deficiency of Fan, stating:

[1] Figures 3 and 4 of Fan include an apparent typographical error regarding the reference numeral (29) associated with the "LOWPASS FILTER," which is associated with the reference numeral (129) in the specification. *See*, e.g., column 4, lines 43-44.

> Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a {sic} larger capacitor for the well known purpose of optimizing the value of the capacitance.

Id. However, Figure 6.17 of Riedel merely discloses the well known rule that a plurality of capacitors connected in series is equivalent to a single capacitor, the admittance 1/Ceq of which is equal to the sum $1/C1 + 1/C2 + \ldots + 1/Cn$ of the admittances of the plurality. More particularly, such disclosure of Riedel is irrelevant to the deficiency of Fan of a series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator.

Referring to the Advisory Action Before Filing of an Appeal Brief dated January 21, 2009, the examiner briefly states "C1 and C3 are series capacitors coupling the phase comparator and the VCO as stated in the rejection." However, in Figure 6 of Fan, capacitors C1 and C3 are clearly connected to ground and would be considered as "parallel capacitors" by one of ordinary skill in the art. Therefore, the examiner's assertion that the capacitors (C1 and C3) disclose the series capacitors recited by claims 1, 7, and 10-14 is clearly in error.

Further, none of the other applied references supplies these deficiencies of Fan and Riedel.

Therefore, because none of the applied references discloses or suggests the series voltage shift capacitor, as recited by claims 1, 7, and 10-14, it is evident that the claims are not obvious thereover and the applicants respectfully request withdrawal of the pending rejections and allowance of claims 1, 7, and 10-14.

B. Claims 1, 7, and 10-14 are not obvious over Fan in view of Riedel because Fan and Riedel do not disclose or suggest controlled polarization means designed to ensure the polarization of an input during the pre-charging of the voltage shift capacitor.

The applicants traverse the argument in the Office action that the 1-bit quantizer (40)

shown in Figure 4 of Fan discloses controlled polarization means, because there is no disclosure in Fan that the 1-bit quantizer (40) is designed to ensure the polarization of an input of a voltage shift control circuit, as recited by the claims at issue.

Rather, the examiner identifies the "input" recited by the claims at issue as the "input of the charge pump A." Office action at page 2. Referring to Figures 3 and 4 of Fan, the 1-bit quantizer (40) is included in the low pass filter (29/129)[2] and is further coupled to the switch (Sb) of the charge pump (28) to control same. There is no disclosure in Fan that the 1-bit quantizer (40) has any impact on the polarization of the input to the charge pump A. For this additional reason, claims 1, 7, and 10-14 are not disclosed or suggested by the applied references and the applicants respectfully request withdrawal of the pending rejections and allowance of claims 1, 7, and 10-14..

C. Dependent claims 2-5, 8, and 9 are not obvious over Fan in view of Kumar in further view of Riedel.

Claims 2-5, 8, and 9 are allowable for at least the same reasons presented in sections 7(A) and 7(B) hereinabove because such claims are dependent upon independent claim 1 and stand or fall with independent claim 1. Therefore, the pending obviousness rejections of claims 2-5, 8, and 9 over Fan in view of Kumar and Riedel should be withdrawn by the Board, notice of which is respectfully requested.

D. Conclusion

Because the applied references do not disclose or suggest all of the elements recited by the claims at issue, it follows that such claims are not rendered obvious thereby. Therefore, applicants respectfully request withdrawal of all pending grounds of rejection and allowance of the claims at issue.

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[2] See footnote 1, above.

Respectfully submitted,

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(8) Claims appendix

The claims stand as amended by Amendment A filed March 25, 2008.

1. Voltage shift control circuit intended to be placed in parallel with at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop and comprising:

- an input, intended to be coupled with the output of the phase comparator;
- an output, intended to be coupled with the input of the voltage controlled oscillator;
- controlled charging means, designed to charge the voltage shift capacitor according to a control signal;
- controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and
- controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

2. Circuit according to Claim 1, wherein the controlled charging means comprise a first operational amplifier connected as a voltage follower between the input and the output, a resistor placed in the feedback loop of the operational amplifier, and a controlled current source supplying a current of specified value through said resistor.

3. Circuit according to Claim 2, wherein the operational amplifier of the charging means comprise a push-pull output stage, and wherein the charging means further comprise a resistor of high value connected in series between the output of the operational amplifier and the output of the circuit.

4. Circuit according to Claim 3, wherein the controlled pre-charging means comprise a push-pull stage which, in the activation of the pre-charging means configuration, is arranged as a mirror with respect to the push-pull output stage of the operational amplifier of the charging means, in such a way as to short-circuit the high value resistor.

5. Circuit according to Claim 4, wherein the push-pull stage of the pre-charging means is designed to deliver a current higher than the current delivered by the push-pull output stage of the operational amplifier of the charging means.

6. Circuit according to Claim 1, wherein the controlled polarization means comprise a second operational amplifier connected as a voltage follower which, in the activation of the controlled polarization means configuration, is arranged to impose a common mode voltage on the input of the circuit.

7. Circuit according to Claim 1, further comprising means for deactivating the controlled pre-charging means before the controlled polarization means.

8. Circuit according to Claim 2, further comprising an additional controlled push-pull stage whose output is intended to be connected to the centre point of an RC network of a loop filter of the PLL and which, in the activation configuration, is connected as a mirror with respect to the push-pull stage of the controlled pre-charging means and with respect to the push-pull output stage of the operational amplifier of the charging means.

9. Circuit according to Claim 8, wherein the additional controlled push-pull stage is integrated with the operational amplifier of the charging means.

10. Circuit according to Claim1, designed in CMOS technology.

11. Phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a series voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the series voltage shift capacitor and comprising:

- an input, intended to be coupled with the output of the phase comparator;
- an output, intended to be coupled with the input of the voltage controlled oscillator;
- controlled charging means, designed to charge the voltage shift capacitor according to a control signal;
- controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and
- controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

12. Radio-frequency transmitter, having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a series voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the series voltage shift capacitor and comprising:

- an input, intended to be coupled with the output of the phase comparator;
- an output, intended to be coupled with the input of the voltage controlled oscillator;
- controlled charging means, designed to charge the voltage shift capacitor according to a control signal;
- controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and
- controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

13. Mobile terminal of a radio-communications system with a radio-frequency transmitter having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a series voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to claim 1 placed in parallel with the series voltage shift capacitor and comprising:

- an input, intended to be coupled with the output of the phase comparator;
- an output, intended to be coupled with the input of the voltage controlled oscillator;
- controlled charging means, designed to charge the voltage shift capacitor according to a control signal;
- controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and
- controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

14. Base station of a radio-communications system with a radio-frequency transmitter having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a series voltage shift control circuit according to Claim 1 placed in parallel with series the voltage shift capacitor and comprising:

- an input, intended to be coupled with the output of the phase comparator;
- an output, intended to be coupled with the input of the voltage controlled oscillator;
- controlled charging means, designed to charge the voltage shift capacitor according to a control signal;
- controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and
- controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

(9) Evidence appendix

-- none --

(10) Related proceedings appendix

-- none --